

# TSM40N03PQ56 30V N-Channel Power MOSFET



#### PDFN56

# 8

#### Pin Definition:

1. Source	8. Drair
2. Source	7. Drair
3. Source	6. Drair
4. Gate	5. Drair

#### PRODUCT SUMMARY

V <sub>DS</sub> (V)	$R_{DS(on)}(m\Omega)$	I <sub>D</sub> (A)
20	4.5 @ V <sub>GS</sub> =10V	19
30	5.8 @ V <sub>GS</sub> =4.5V	16

### **Features**

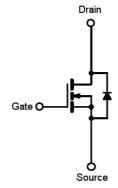
- Advanced Trench Technology
- Low On-Resistance
- Low gate charge typical @ 12nC (Typ.)
- Low Crss typical @ 140pF (Typ.)

## **Ordering Information**

Part No.	Package	Packing
TSM40N03PQ56 RLG	PDFN56	2.5Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

## **Block Diagram**



N-Channel MOSFET

## **Absolute Maximum Ratings** (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		$V_{DS}$	30	V	
Gate-Source Voltage	Gate-Source Voltage		±20	V	
	T <sub>C</sub> =25°C		40		
Continuous Drain Current	T <sub>C</sub> =70°C	,	40	Α	
	T <sub>A</sub> =25°C	l <sub>D</sub>	31		
	T <sub>A</sub> =70°C		25		
Drain Current-Pulsed Note 1		I <sub>DM</sub>	100	Α	
Avalanche Current, L=0.5mH		I <sub>AS</sub> , I <sub>AR</sub> 38		Α	
Avalanche Energy, L=0.5mH		E <sub>AS</sub> , E <sub>AR</sub>	72	mJ	
	T <sub>C</sub> =25°C		36		
Maximum Power Dissipation	T <sub>C</sub> =70°C	Б	23	W	
	T <sub>A</sub> =25°C	$P_{D}$	4.2		
	T <sub>A</sub> =70°C		2.7		
Storage Temperature Range		T <sub>STG</sub>	-55 to +150	°C	
Operating Junction Temperature Range		$T_J$	-55 to +150	°C	

<sup>\*</sup> Limited by maximum junction temperature

#### **Thermal Performance**

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	R⊖ <sub>JC</sub>	3.5	°C/W
Thermal Resistance - Junction to Ambient	RO <sub>JA</sub>	30	°C/W

Notes: Surface mounted on FR4 board t ≤ 10sec

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## **TSM40N03PQ56**



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## **Electrical Specifications** (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV <sub>DSS</sub>	30			V
Drain-Source On-State Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 19A	Б		3.5	4.5	mΩ
	$V_{GS} = 4.5V, I_D = 16A$	$R_{DS(ON)}$		4.6	5.8	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	$V_{GS(TH)}$	1.15		2.2	V
Zero Gate Voltage Drain Current	$V_{DS} = 24V, V_{GS} = 0V$	I <sub>DSS</sub>			1	μΑ
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I <sub>GSS</sub>	-		±100	nA
Dynamic						
Total Gate Charge		$Q_g$	-	12		
Gate-Source Charge	$V_{DS} = 15V, I_D = 19A,$	$Q_{gs}$		5.4		nC
Gate-Drain Charge	V <sub>GS</sub> = 4.5V	$Q_{gd}$	I	4.6		
Input Capacitance	\/ - 45\/ \/ - 0\/	C <sub>iss</sub>	I	1700		
Output Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ f = 1.0MHz	C <sub>oss</sub>	I	350		pF
Reverse Transfer Capacitance	1 = 1.0WIDZ	C <sub>rss</sub>	I	140		
Switching						
Turn-On Delay Time		t <sub>d(on)</sub>		25		
Turn-On Rise Time	$V_{GS} = 4.5V, V_{DS} = 15V,$	t <sub>r</sub>		20		
Turn-Off Delay Time	$R_G = 1\Omega$	$t_{d(off)}$		25		ns
Turn-Off Fall Time		t <sub>f</sub>		15		
Drain-Source Diode Characteristic	s and Maximum Rating					
Drain-Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	V <sub>SD</sub>	-	0.8	1.2	٧
Reverse Recovery Time	I <sub>S</sub> = 10A, T <sub>J</sub> =25 °C	t <sub>fr</sub>	-	25		ns
Reverse Recovery Charge	dl/dt = 100A/µs	Q <sub>fr</sub>		17		nC

### Notes:

- 1. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 2.  $R\theta_{JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R\theta_{JC}$  is guaranteed by design while  $R\theta_{CA}$ is determined by the user's board design. Rθ<sub>JA</sub> shown below for single device operation on FR-4 in still air

3. The maximum current rating is limited by package.

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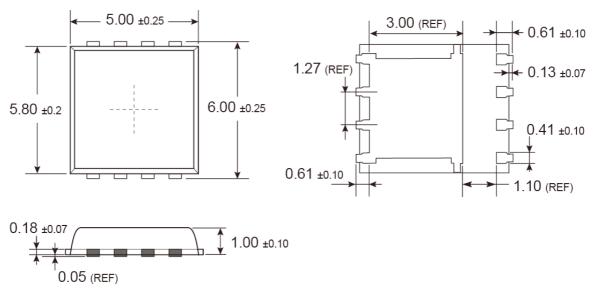


## **TSM40N03PQ56**

## 30V N-Channel Power MOSFET



## **PDFN56 Mechanical Drawing**



**Unit: Millimeters** 

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## TSM40N03PQ56 30V N-Channel Power MOSFET

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